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Information Technology

Fibre Channel - High-Speed Parallel Interface

Draft proposed Technical Report

Secretariat of the National Committee for Information Technology Standardization (NCITS)

ABSTRACT

This technical report defines the functions and electrical characteristics of the high-speed parallel interface between the physical (FC-0) layer and the transmission protocol (FC-1) layer of a Fibre Channel port. This interface operates at either 2 125,0 or 1 062,5 Mbaud. This interface has additional functions and different electrical characteristics compared to the “Fibre Channel - 10-bit Interface”, previously published as X3.TR-18:1997, which operated at 1 062,5 MBaud only. This document applies in full to systems where the FC-0 and FC-1 layer are implemented as separate devices. For systems where the FC-0 and FC-1 devices are integrated, only the functional characteristics of this document apply.

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REVISION HISTORY

Revision	Date	Comment
1	Dec/1/98	As released
2	Jan/29/99	Reformatted into one column per current T11 policy Elimination of -LCK_REF signal Defined static output state for EWRAP signal Added RX_LOS signal (detailed specs in FC-PI) Defined Tx[0:9]/TBC timing in 1G mode (negative edge of TBC will be used) Defined RBC[0:1] frequency in 1G mode (53 MHz) Added PECL voltage specs for REFCLK Changed VREFI to VREFT (T=Transmit) and VREFO to VREFR (R=Receive)
2.1	Feb/3/99	Fixed error in RX_LOS spec (inverted signal)
3	Apr/5/99	Changed VREFR in Figure 1 to go to FC-1 device instead of to PCB Added TBC wander spec (90 degrees from REFCLK[0:1]) to section 4.2.2 (TBC) Changed Section 4.2.3 and Table 1 to make clear that REFCLK is active when REFCLK[1] is high Changed Iih_SSTL and Iil_SSTL max in Table 2 to +/- 100uA (from +250/-150uA before) Added IVREFR spec (40 uA min) to Table 2 and set IVREFT to 40 uA max Added min/max frequency (approx. +/- 3%) to RBC spec (Tables 6 and 7) Added Ttxct spec (0.2 UI) to bound Tx[0:9]/TBC transition time when operating at 2 125 MBaud Added several specs to Table 3 Deleted original Figure 2; it was not adding useful information Added a new Figure 2 to show active edge and timing of REFCLK[0:1] Added sentence to 4.2.13 which forces VREFR to be able to drive at least one VREFT input (also shown with numbers in Table 2) Added reference to GBIC document in section 4.2.14 (RX_LOS) Changed Vih_PECL and Vil_PECL levels in Table 3 Minor typography changes
4	May/26/99	Changed Schelto's company to Infineon Technologies on page ii Added text to ABSTRACT (page i) and Scope (page 4) to indicate that this document applies in full to discrete FC-0/FC-1 devices and that only the functional characteristics of this document apply to integrated FC-0/FC-1 designs Added text to 4.2.2 (TBC) indicating that maintenance of the required +/- 90 degree phase relationship between TBC and REFCLK[0:1] is vendor-dependent Added SSTL_2 spec pointer to section 5.1 regarding unterminated inputs on SSTL_2 lines Made various changes to Conditions column in Table 2 Made clear that clock and data rise and fall times in Tables 2 and 3 are measured at the receiving device and aren't affected by the unterminated transmission line step Added new section 5.1.2 to describe SSTL_2 output AC test circuit Created new Figure 2 and renumbered subsequent figures accordingly

4.1	Jun/8/99	Minor typography changes.
5	Jul/20/99	Letter ballot comment resolutions included. See 99-425v0.pdf for more details on the comments.
5.1	Aug/2/99	Includes modifications to letter ballot comment resolutions in Sections 5.1.1 and 5.2 taken at Rochester FC-HSPI meeting.

1 Scope

This document defines the functions and electrical characteristics of a High-Speed Parallel Interface between FC-1 (Transmission protocol layer) and FC-0 (Physical layer) devices at 2 125,0 and 1 062,5 MBaud data rates. This document applies in full to systems where the FC-0 and FC-1 layer are implemented as separate devices. For systems where the FC-0 and FC-1 devices are integrated, only the functional characteristics of this document apply.

The High-Speed Parallel Interface is composed of two subinterfaces: Transmit Interface and Receive Interface. Figure 1 shows the relationship of these interfaces.

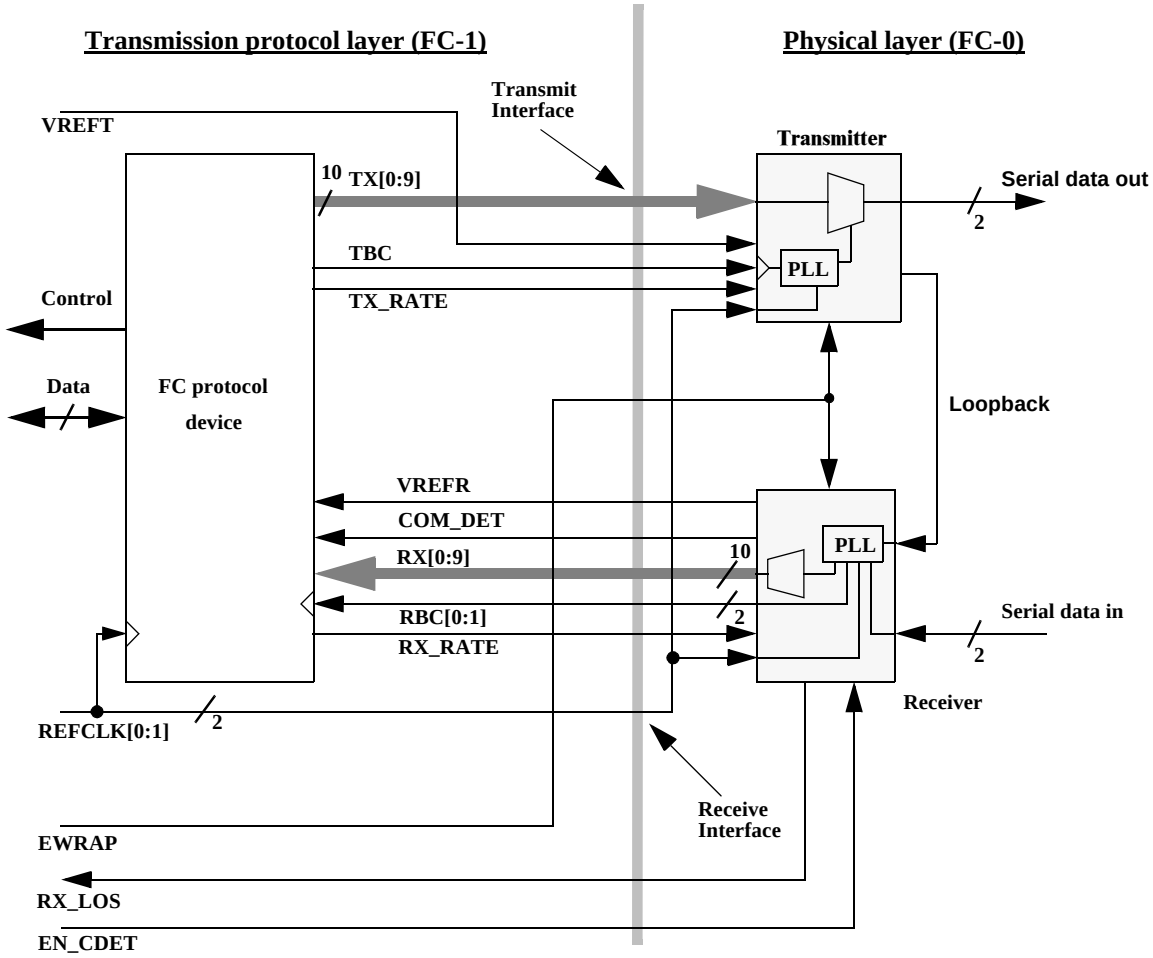

FIGURE 1 - HIGH-SPEED PARALLEL INTERFACE DIAGRAM

2 Normative references

The following American National Standards contain provisions which, through reference below, constitute provisions of this Technical Report. All standards are subject to revisions, and parties to agreements based on this Technical Report are encouraged to apply the most recent editions of the standards. Members of IEC and ISO maintain registers of currently valid International Standards. ANSI performs a similar function for American National Standards.

ANSI X3.230-199x, *Fibre Channel Physical Interface (FC-PI)*
ANSI X3.230-199x, *Fibre Channel Framing and Signaling Interface (FC-FS)*

3 Definitions and conventions

The following definitions, conventions, abbreviations, acronyms and symbols apply in addition to those in *FC-PI* and *FC-FS*.

3.1 Definitions

3.1.1 byte alignment: The receiver action that resets the byte boundary to the comma within the K28.5 character being received.

3.1.2 byte slipping: The receiver action that eliminates the 180° phase error between the receive data and the receive byte clock.

3.1.3 comma+: The seven bit sequence (0011111) of an encoded data stream.

3.1.4 comma-: The seven bit sequence (1100000) of an encoded data stream.

3.1.5 sliver: A pulse with a duration which is less than that specified for that signal (e.g. a truncated clock signal).

3.1.6 word alignment: The process by which an entity determines the location of the four byte (“word”) boundary in a continuous byte stream.

3.2 Editorial conventions

In this Technical Report, a number of conditions, mechanisms, sequences, parameters, event states, or similar terms are printed with the first letter of each word in uppercase and the rest in lowercase (e.g. Physical). Any lowercase uses of these words have the normal technical English meaning.

Numbered items in this Technical Report do not represent any priority. Priority, if it exists, is explicitly indicated.

The ISO convention of numbering is used. The thousands and higher multiples are separated by a space and a comma is used as the decimal point. A comparison of the American and ISO conventions are shown:

ISO	American
0,1	0.1
1 234	1,234
1 234 567,8	1,234,567.8

In case of conflict between figures, tables, and text, the text shall take precedence. Exceptions to this convention are indicated if appropriate.

In figures, tables, and text, the most significant bit of a binary quantity is shown on the left side. Exceptions to this convention are indicated if appropriate.
The term “shall” is used to indicate a mandatory rule. If the mandatory rule is not followed, the results are unpredictable unless indicated otherwise.
If a field or control bit in a frame is specified as not meaningful, the entity which receives the frame shall not check that field or control bit.

Hexadecimal notation is used to represent fields. For example, a three byte D_ID field containing a binary value of 11111111 11111111 11111010 is denoted by FF FF FA.

3.3 Abbreviations, acronyms and symbols

The following abbreviations and acronyms are applicable to this Technical Report.

FC	Fibre Channel
PLL	Phase Locked Loop
ppm	parts per million

4 Functional description

The Transmit Interface is defined as an input to the Physical layer device with a 10-bit wide transmit data bus (Tx[0:9]), its associated transmit byte clock (TBC) and a speed selector (TX_RATE). The reference clock is a differential 106,25 MHz ±100 ppm signal (REFCLK[0:1]). REFCLK[0:1] frequency is independent of both the Transmit Interface and Receive Interface data rates. The Transmission protocol layer device presents data to the Physical layer device relative to the falling edge of TBC when the Transmit Interface is operating at 1 062,5 MBaud. The Transmission protocol layer device presents data to the Physical layer device synchronous with both rising and falling edges of TBC when the Transmit Interface is operating at 2 125,0 MBaud. The speed of the Transmit Interface is set by the TX_RATE signal. A transmit reference voltage (VREFT) is provided to ensure that TBC and Tx[0:9] have a well-defined threshold between low and high values in order to reduce jitter.

The Receive Interface is defined as an output of the Physical layer device with a 10-bit wide data bus (Rx[0:9]), two receive byte clocks (RBC[0:1]), an optional comma detection enable (EN_CDET), a comma detection indication (COM_DET) and a speed selector (RX_RATE). The receive byte clocks operate at 53,125 MHz when the Receive Interface data rate is 1 062,5 MBaud and at 106,25 MHz when the Receive Interface data rate is 2 125,0 MBaud. The receive byte clocks are 180° out of phase with each other. Receive data is presented to the Transmission protocol layer device relative to the rising edge of each of RBC[0] and/or RBC[1]. The speed of the Receive Interface is set by the RX_RATE signal. A receive reference voltage (VREFR) is provided to ensure that RBC[0:1] and Rx[0:9] have well-defined threshold between low and high values in order to reduce jitter.

Two additional signals complete the definition of the High-Speed Parallel Interface. The first is the wrap or loopback signal (EWRAP). This signal is defined as an input to the Physical layer device which causes serialized transmit data to be looped back to the auxiliary inputs of the receiver deserializer. The second is receiver loss-of-signal (RX_LOS). This signal indicates when the amplitude of the incoming serial data is low enough to be considered invalid.

4.1 Data flow

The 10-bit data presented to the Physical layer device shall be serially transmitted to the cable plant, bits Tx[0]-Tx[9] sequentially. The relationship of transmit bits and the 10-bit 8B/10B-encoded characters is described in *FC-FS*.

The receiver in the Physical layer device shall receive and frame data at an arbitrary byte boundary until a comma sequence is received. The receiver shall realign its current byte boundary, if necessary, to that of the received comma. This process is called “byte alignment”. During the byte alignment process the Physical layer device may delete up to 4 characters in order to align the receive clock and the data byte containing the comma character (byte 0). This process is called “byte slipping”.

4.2 Electrical interface signals

The Transmit Interface and Receive Interface signals listed below shall comprise the minimum set of signals which must be supplied for compliance with this Technical Report. Each signal is described in its own subsection which is headed with the signal name followed by the logic family in parentheses. In case of conflict between specifications in this document and other documents describing similarly-named logic families, this document shall take precedence. The two static reference voltage signals do not have associated logic families. Electrical signal levels are described in Section 5.

4.2.1 Tx[0:9] (SSTL_2)

Tx[0:9] is the 10-bit parallel transmit data presented to the Physical layer device for serialization and transmission onto the media. The order of transmission is Tx[0] first, followed by Tx[1] through Tx[9]. If the Transmit Interface is operating at 2 125,0 MBaud, Tx[0:9] shall be 212,50 MBaud. If the Transmit Interface is operating at 1 062,5 MBaud, Tx[0:9] shall be 106,25 MBaud.

4.2.2 TBC (SSTL_2)

TBC is the transmit byte clock which operates at 106,25 MHz independent of the Transmit Interface data rate. TBC is used to read data into the Physical layer device for transmission. When the Transmit Interface is operating at 2 125,0 MBaud, TBC shall be synchronous with Tx[0:9] (“source-synchronous”) and data shall be read into the Physical layer device on both edges of TBC. When the Transmit Interface is operating at 1 062,5 MBaud, data shall be read into the Physical layer device on the falling edge of TBC. TBC shall be frequency locked to REFCLK[0:1]. The phase relationship of TBC to REFCLK[0:1] must be maintained within +/- 90 degrees and is vendor-dependent.

4.2.3 REFCLK[0:1] (PECL)

REFCLK[0:1] is the differential 106,25 MHz transmit PLL reference clock. The frequency tolerance for this clock shall be ±100 ppm. REFCLK[0:1] may be used by the transmitter PLL to generate the 2 125,0 or 1 062,5 MHz bit rate clocks used in serial data transmission. Receivers shall automatically lock to REFCLK[0:1]. REFCLK[0:1] is active on the rising edge of REFCLK[1].

4.2.4 TX_RATE (SSTL_2)

TX_RATE is the speed selector for the Transmit Interface. When TX_RATE is set to logical 0, the Transmit Interface shall operate at 1 062,5 MBaud. When TX_RATE is set to logical 1, the Transmit Interface shall operate at 2 125,0 MBaud.

4.2.5 VREFT

VREFT is the reference voltage for Tx[0:9], TBC, TX_RATE, RX_RATE, EWRAP and EN_CDET. The Physical layer device shall interpret Tx[0:9], TBC, TX_RATE, RX_RATE, EWRAP and EN_CDET as logical 1 when their voltages are greater than VREFT. The Physical layer device shall interpret Tx[0:9], TBC, TX_RATE, RX_RATE, EWRAP and EN_CDET as logical 0 when their voltages are less than VREFT. VREFT may be supplied by the Transmission protocol layer device.

4.2.6 Rx[0:9] (SSTL_2)

Rx[0:9] is the 10-bit parallel receive data presented to the Transmission protocol layer device for further processing. Data byte 0 of a four-byte receive word containing the comma character shall be byte aligned to RBC[1] (byte 0 is in phase with RBC[1]).

4.2.7 RBC[0] (SSTL_2)

RBC[0] is the receive byte clock. On the rising edge of RBC[0], the Transmission protocol layer device shall latch bytes 1 and 3 of the receive data word. RBC[0] is 53,125 MHz when the Receive Interface is operating at 1 062,5 MBaud. RBC[0] is 106,25 MHz when the Receive Interface is operating at 2 125,0 MBaud. RBC[0] may be stretched during byte and word alignment. RBC[0] shall not be truncated or slivered.

4.2.8 RBC[1] (SSTL_2)

RBC[1] is the receive byte clock. On the rising edge of RBC[1], the Transmission protocol layer device shall latch bytes 0 and 2 of the receive data word. RBC[1] is 53,125 MHz when the Receive Interface is operating at 1 062,5 MBaud. RBC[1] is 106,25 MHz when the Receive Interface is operating at 2 125,0 MBaud. RBC[1] is 180° out of phase with RBC[0]. RBC[1] may be stretched during byte and word alignment. RBC[1] shall not be truncated or slivered.

4.2.9 EWRAP (SSTL_2)

EWRAP shall cause the Physical layer device to electrically loop serialized transmit data to the deserializer. The primary serial outputs on the transmitter shall be held in a static state during EWRAP operation. EWRAP may be tied to logical 0 (disabled) by the Transmission protocol layer device.

4.2.10 COM_DET (SSTL_2)

COM_DET is an indication that the data byte (byte 0 of word 0) associated with the current RBC[1] contains a valid comma character. The Physical layer device shall be required, as a minimum, to detect the 7-bit comma+ character. The Physical layer device shall provide this signal as an output but the Transmission protocol layer device may optionally ignore COM_DET.

4.2.11 EN_CDET (SSTL_2)

EN_CDET enables the Physical layer device to perform the byte alignment function on the comma sequence. When EN_CDET is asserted the byte alignment function is operational. The Physical layer device may have the byte alignment function always enabled.

4.2.12 RX_RATE (SSTL_2)

RX_RATE is the speed selector for the Receive Interface. When RX_RATE is set to logical 0, the Receive Interface shall operate at 1 062,5 MBaud. When RX_RATE is set to logical 1, the Receive Interface shall operate at 2 125,0 MBaud.

4.2.13 VREFR

VREFR is the reference voltage for Rx[0:9], RBC[0:1], COM_DET and RX_LOS. The Transmission protocol layer device shall interpret Rx[0:9], RBC[0:1], COM_DET and RX_LOS as logical 1 when their voltages are greater than VREFR. The Transmission protocol layer device shall interpret Rx[0:9], RBC[0:1], COM_DET and RX_LOS as logical 0 when their voltages are less than VREFR. VREFR may be supplied from the Physical layer device. VREFR must have at least enough current sourcing and sinking capability to drive one VREFT input (see Table 2).

4.2.14 RX_LOS (SSTL_2)

RX_LOS is the receiver loss-of-signal indicator. When the amplitude of the incoming high-speed serial data is too low for that data to be considered valid, RX_LOS shall be set to logical 1. Details on timing of RX_LOS and the voltage levels of the incoming high-speed serial data required to set RX_LOS may be found in *FC-PI*.

4.3 Signal definitions

The signals shown in Table 1 shall be required at the High-Speed Parallel Interface but all signal functions may not be utilized by the Physical or Transmission protocol layer devices.

TABLE 1 - SIGNAL DEFINITIONS

Symbol	Signal Name	Signal Type[1]	Active Level
Tx[0:9]	Transmit Data	Input	L/H
TBC	Transmit Byte Clock	Clock Input	Rising and falling edges (see Section 4.2.2)
REFCLK[0:1]	Reference Clock	Clock Input	Rising edge of REFCLK[1] (see Section 4.2.3)
TX_RATE	Transmit Interface Speed Select	Input	L/H
VREFT	Transmit Reference Voltage	Input	Static
Rx[0:9]	Receive Data	Output	L/H
RBC[0]	Receive Clock	Clock Output	Rising edge (see Section 4.2.7)
RBC[1]	Receive Clock	Clock Output	Rising edge (see Section 4.2.8)
EWRAP	Enable Wrap (Loopback)	Input	H
COM_DET	Comma Detect	Output	H
EN_CDET	Enable Comma Detect	Input	H
RX_RATE	Receive Interface Speed Select	Input	L/H
VREFR	Output Reference Voltage	Output	Static
RX_LOS	Receiver Loss-of-Signal Indication	Output	H

[1] Defined relative to the Physical layer device.

5 Electrical definitions

5.1 SSTL_2 characteristics

Table 2 documents the required DC and AC parametric attributes of all SSTL_2 inputs to and outputs from the Physical layer device. Input levels to the Physical layer device may be greater than the power supply level and Physical layer devices may tolerate such inputs. All SSTL_2 inputs are assumed to be unterminated per Section 4.1 of the SSTL_2 specification. For reference, the SSTL_2 specification is available from http://www.jedec.org/DOWNLOAD/freeStd/jesd8-xx/JESD8-9.PDF. In case of conflicts between specifications in this document and the SSTL_2 standard, this document shall take precedence.

TABLE 2 - SSTL_2 ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VREFT	Transmit Reference Voltage		1,15	1,25	1,35	V
VREFR	Receive Reference Voltage	|IVREFR| ≤ 40µA	1,15	1,25	1,35	V
$\|I_{VREFT}\|$	VREFT Input Current	1,15V ≤ VREFT ≤ 1,35V			40	µA
$\|I_{VREFR}\|$	VREFR Input Current	1,15V ≤ VREFR ≤ 1,35V			40	µA
V_{OH_SSTL}	Output High Voltage		VREF[T|R] + 0,38		V_{CC} + 0,3	V
V_{OL_SSTL}	Output Low Voltage		-0,3		VREF[T|R] - 0,38	V
V_{IH_SSTL}	Input High Voltage		VREF[T|R] + 0,35		V_{CC}[1] + 0,3	V
V_{IL_SSTL}	Input Low Voltage		-0,3		VREF[T|R] - 0,35	V
I_{IH_SSTL}	Input High Current	$V=V_{IH\_SSTL(max)}$			100	µA
I_{IL_SSTL}	Input Low Current	$V=V_{IL\_SSTL(min)}$			-100	µA
C_{IN}	Input Capacitance				4,0	pF
t_R	Clock and Data Rise Time (at receiving device)	VREF[T|R] - 0,35V to VREF[T|R] + 0,35V			1,5	ns
t_F	Clock and Data Fall Time (at receiving device)	VREF[T|R] + 0,35V to VREF[T|R] - 0,35V			1,5	ns

[1] Refers to the driving device power supply.

5.1.1 Valid signal levels

All AC measurements are made from the reference voltage level (VREFT for Transmit Interface and VREFR for Receive Interface) of the clock to the valid input or output data levels. The valid input and output data levels are 0,35V away from VREF[T|R] and are different than those used in the SSTL_2 specification. All AC measurements are assumed to have an output load of 4,0 pF.

5.1.2 SSTL_2 output AC test circuit

Figure 2 shows a recommended circuit for testing compliance to the SSTL_2 output specifications of Table 2. This circuit is designed to be implementable in an automated test environment. The circuit is also similar to standard in-circuit usage of the SSTL_2 outputs.

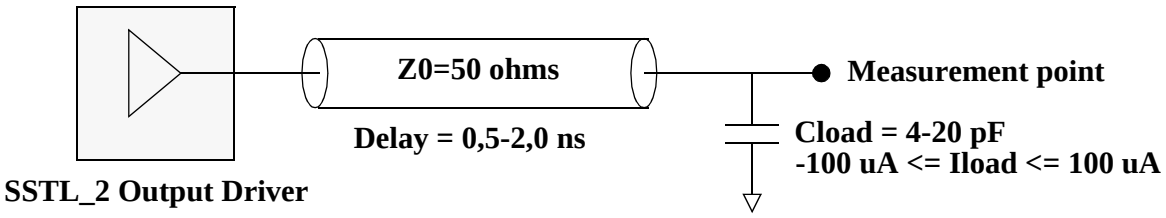

FIGURE 2 - SSTL_2 OUTPUT AC TEST CIRCUIT

5.2 PECL electrical characteristics

Table 3 and Figure 3 document the required DC and AC attributes of all PECL inputs to the Physical layer device. Although these signals are labeled PECL, this is not a clearly defined logic standard. In case of conflicts between specifications in Table 3 and other documents describing similarly-named logic families, Table 3 shall take precedence. Input levels to the Physical layer device may be greater than the power supply level and Physical layer devices may tolerate such inputs.

TABLE 3 - REFCLK[0:1] ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH_PECL}	REFCLK[0:1] Input High Voltage		2,1		2,6	V
V_{IL_PECL}	REFCLK[0:1] Input Low Voltage		1,3		1,8	V
f_{REFCLK}	REFCLK[0:1] Frequency		106,25 - 100 ppm	106,25	106,25 + 100 ppm	MHz
t_{R_PECL}	REFCLK[0:1] Rise Time (at receiving device)	$V_{IL\_PECL(max)}$ to $V_{IH\_PECL(min)}$			1,5	ns
t_{F_PECL}	REFCLK[0:1] Fall Time (at receiving device)	$V_{IH\_PECL(min)}$ to $V_{IL\_PECL(max)}$			1,5	ns
	REFCLK[0:1] Duty Cycle	50% point to 50% point	40		60	%
t_{TBC_REFCLK}	TBC to REFCLK[0:1] Skew	50% point to 50% point			2,35	ns

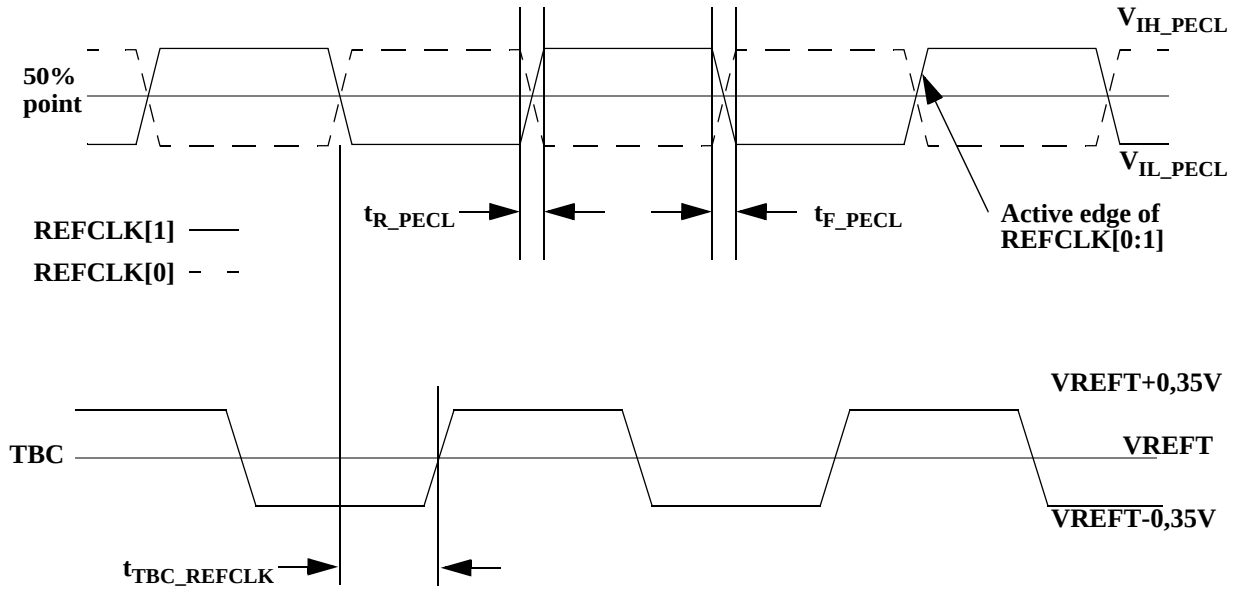

FIGURE 3 - REFCLK[0:1] TIMING AND TBC PHASE RELATIONSHIP

6 Transmit Interface

6.1 Transmit data (Tx[0:9])

The Tx[0:9] signals carry data from the Transmission protocol layer device to the Physical layer device to be transmitted onto the media. Refer to *FC-FS* for the proper transmission order. All 10-bit data presented to the Physical layer device shall conform to the 8B/10B code as specified in *FC-FS*.

6.2 Transmit reference voltage generation

Any method of generating the Input Reference Voltage (VREFT) may be used as long as the specifications of Table 2 are met. For best results, VREFT should track variations in the Transmission protocol layer device supply voltage. VREFT may be generated by the Transmission protocol layer device.

6.3 Transmit Interface timing

At 1 062,5 MBaud, the Transmit Interface uses ordinary edge clocking. The falling edge of TBC is used to clock Tx[0:9] into the Physical layer device. However, the Transmit Interface uses “source-synchronous” clocking when operating at 2 125,0 MBaud. “Source-synchronous” refers to the fact that TBC and Tx[0:9] are synchronous at the Transmission protocol layer device. This kind of interface is popular in synchronous DRAMs and other devices where high bus speeds are necessary. TBC can be thought of as an always-transitioning eleventh data bit when the Transmit Interface is source-synchronous and the usual concepts of Tx[0:9] setup and hold time don’t apply when observing Tx[0:9] and TBC at the input to the Physical layer device. Source-synchronous clocking, while not strictly necessary at the 106,25 MHz Transmit Interface bus speed, will become critical as the Transmit Interface bus speed scales up in future implementations of FC-HSPI.

The Transmit Interface The Transmit Interface timing specified in Figures 4-5 and in Tables 4-5 defines the Physical layer device input. All transitions in Figures 4-5 are specified from the TBC reference level (VREFT) to valid input signal levels.

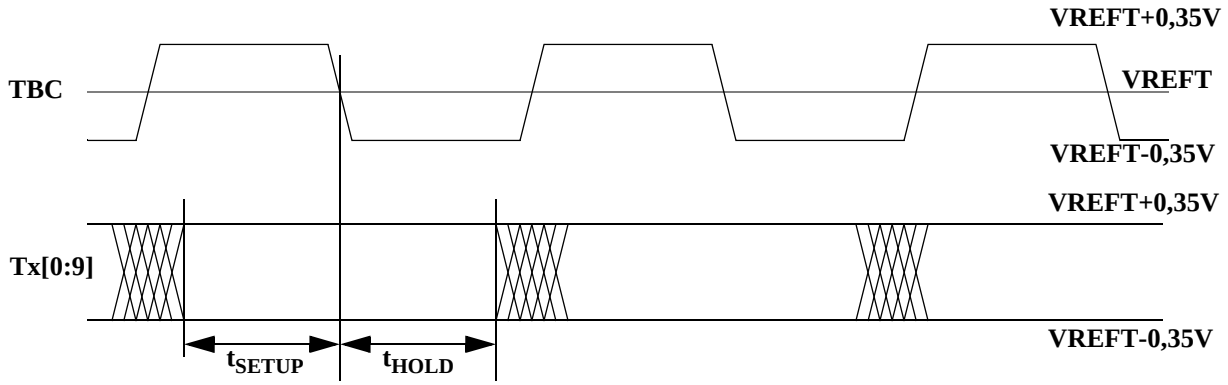

FIGURE 4 - TRANSMIT INTERFACE TIMING DIAGRAM WHEN TRANSMIT INTERFACE IS OPERATING AT 1 062,5 MBAUD

TABLE 4 - TRANSMIT INTERFACE TIMING WHEN TRANSMIT INTERFACE IS OPERATING AT 1 062,5 MBAUD

Parameter	Description	Min	Typ	Max	Units
f_{TBC}	TBC Frequency	106.25 - 100 ppm	106.25	106.25 + 100 ppm	MHz
t_{SETUP}	Data Setup Before TBC Falling Edge	1,4			ns
t_{HOLD}	Data Hold After TBC Falling Edge	1,4			ns

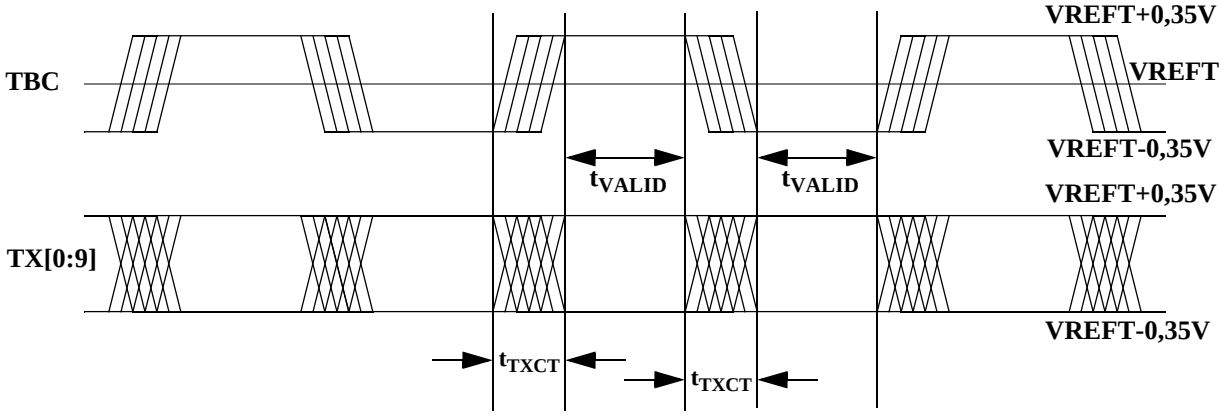

FIGURE 5 - TRANSMIT INTERFACE TIMING DIAGRAM WHEN TRANSMIT INTERFACE IS OPERATING AT 2 125,0 MBAUD

TABLE 5 - TRANSMIT INTERFACE TIMING WHEN TRANSMIT INTERFACE IS OPERATING AT 2 125,0 MBAUD

Parameter	Description	Min	Typ	Max	Units
f_{TBC}	TBC Frequency	106.25 - 100 ppm	106.25	106.25 + 100 ppm	MHz
t_{VALID}	Tx[0:9] Valid Time TBC Valid Time	2.82			ns
t_{TXCT}	Tx[0:9] Transition Time TBC Transition Time			1.88	ns

7 Receive Interface

7.1 Receive data (Rx[0:9])

The Rx[0:9] signals carry parallel data from the Physical layer device receiver to the Transmission protocol layer device for further processing. Byte 0 of the receive data shall be valid during the positive edge of RBC[1]. This provides a method for word alignment for protocol devices not utilizing the comma detect output (COM_DET) from the receiver. All data transferred across this interface shall conform to 8B/10B code as specified in *FC-FS*.

7.2 COM_DET

COM_DET indicates that the Physical layer device receiver has detected a comma sequence and that byte 0 of word 0 associated with the current positive edge of RBC[1] contains a comma character. In order to provide this function, the Physical layer device receiver may delete one or more characters if RBC[1] is out of phase with the received comma sequence. This allows RBC[1] to be stretched an additional one byte (byte slip) so that on the next received comma sequence RBC[1] will be in phase.

The Physical layer device receiver shall detect comma+ (0011111). The Physical layer device receiver may detect two comma sequences (comma+ and comma-) or positive and negative disparity K28.5 characters.

7.3 Receive byte clock (RBC[0:1])

The receive byte clocks are supplied to the protocol device from the Physical layer device receiver and shall be derived from the recovered bit clock. RBC[0] shall be 180° out of phase with RBC[1]. During byte re-alignment the receive byte clocks may be stretched to the new byte boundary and shall not be slivered or truncated.

Tables 6 and 7 specify a receive byte clock drift (t_{DRIFT}) which shall apply under all input conditions to the receiver, including invalid or absent input signals. The receive byte clock drift specification shall not apply when the receiver is aligning to a new byte boundary and RBC[0:1] are being stretched to the new byte boundary. During the alignment process the receive byte clocks slow a fixed amount, depending on the offset of the new comma sequence, and then return to the nominal frequency.

7.4 Receive reference voltage generation

Any method of generating VREFR is acceptable as long as the specifications of Table 2 are met. For best results, VREFR should track variations in the Physical layer device supply voltage. VREFR may be generated by the Physical layer device.

7.5 Receive Interface timing

The Receive Interface timing in Figure 6 and Tables 6-7 defines the Physical layer device output. All transitions in Figure 6 are specified from the RBC[0:1] reference level (VREFR) to valid output signal levels.

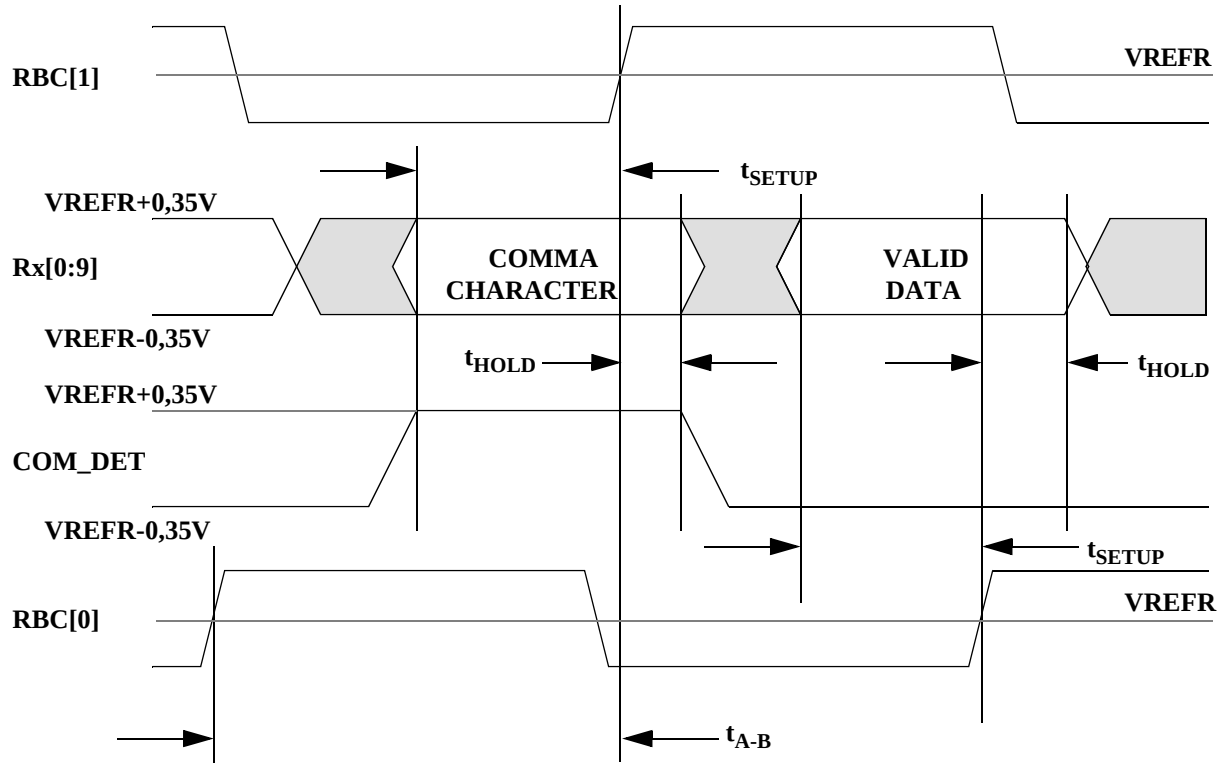

FIGURE 6 - RECEIVE INTERFACE TIMING DIAGRAM WHEN RECEIVE INTERFACE IS OPERATING AT 1 062,5 MBAUD OR AT 2 125,0 MBAUD

TABLE 6 - RECEIVE INTERFACE TIMING WHEN RECEIVE INTERFACE IS OPERATING AT 1 062,5 MBAUD

Parameter	Description	Min	Typ	Max	Units
f_{RBC}	RBC[0:1] Frequency	51,531	53,125	54,719	MHz
t_{DRIFT}	RBC[0:1] Drift Rate[1]	0,2			µs/MHz
t_{SETUP}	Data Setup Before RBC[0:1] Edge	3,0			ns
t_{HOLD}	Data Hold After RBC[0:1] Edge	1,5			ns
t_{DUTY}	RBC[0:1] Duty Cycle	40		60	%
t_{A-B}	RBC[0] to RBC[1] Skew	8,9		9,9	ns

[1] t_{DRIFT} is the minimum time for RBC to drift from 53,5 MHz to 54,5 MHz or from 52,5 MHz to 51,5 MHz. It shall apply under all input signal conditions (except where noted in Section 7.3), including invalid or absent input signals, provided that the receiver PLL was previously locked to REFCLK[0:1] or to a valid input signal.

TABLE 7 - RECEIVE INTERFACE TIMING WHEN RECEIVE INTERFACE IS OPERATING AT 2 125,0 MBAUD

Parameter	Description	Min	Typ	Max	Units
f_{RBC}	RBC[0:1] Frequency	103,06	106,25	109,44	MHz
t_{DRIFT}	RBC[0:1] Drift Rate[1]	0,2			µs/MHz
t_{SETUP}	Data Setup Before RBC[0:1] Edge	1,4			ns
t_{HOLD}	Data Hold After RBC[0:1] Edge	1,4			ns
t_{DUTY}	RBC[0:1] Duty Cycle	40		60	%
t_{A-B}	RBC[0] to RBC[1] Skew	4,5		4,9	ns

[1] t_{DRIFT} is the minimum time for RBC to drift from 107 MHz to 108 MHz or from 105 MHz to 104 MHz. It shall apply under all input signal conditions (except where noted in Section 7.3), including invalid or absent input signals, provided that the receiver PLL was previously locked to REFCLK[0:1] or to a valid input signal.