

TECHNICAL SPECIFICATION

PRELIMINARY DRAFT PROPOSED: MEDIA INTERFACE ADAPTER FOR FIBRE CHANNEL

Abstract:

This document specifies the mechanical, electrical, and signalling requirements for a Media Interface Adapter (MIA) and its corresponding 9-pin D-sub signal interface. This module converts gigahertz electrical signals into modulated light for transmission on optical fibre media. The use of the MIA in applications other than optical conversion is beyond the scope of this specification.

This specification has been developed by a public adhoc committee consisting of representatives of companies who have expressed interest in this subject. Whereas it is the intent to include all such parties, it is realized that not all may have participated. The appearance of the names of companies on the front of this document indicates attendance at one or more adhoc sessions during which this specification was discussed. The appearance of the company name below is not intended to indicate an endorsement of this specification or this design approach by the subject company.

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At present, this effort is conducted independent of affiliation with Committee X3T11. It is anticipated that the output of this effort will be submitted to the appropriate subgroup of X3T11 for consideration as a technical report and/or parts of it may be included within the fibre channel standard.

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Foreword

Continued progress in the FC-AL standard and the Direct Attach Loop Profile effort have caused reemergence of arbitrated loop as an important part of the overall success of fibre channel. This progress in arbitrated loop has spawned numerous new product development, much of it directed toward storage attach and some looking into LAN applications for fibre.

The superior connectivity and bandwidth of Fibre channel are ideally suited for applications in large disk arrays. This market is currently dominated by application of parallel SCSI. Currently expansion is accomplished by the addition of more host adapters to increase the number of SCSI channels. As new applications emerge requiring increasingly more storage and bandwidth, this expansion approach becomes constrained by bandwidth, physical connectivity, PCB space in the host, and machine room floor space. The application of arbitrated loop provides immediate relief to constraints imposed by parallel SCSI. However, if fibre channel is to broaden its appeal for storage attach applications, it must become price competitive with high end parallel SCSI and any other available serial technologies which purport to have application in storage arrays.

The present approach for media adaptation to fibre channel requires a mezzanine GLM (gigabit link module) card containing SERDES and high speed transceiver components. This approach imposes an unnecessary cost and space penalty for copper storage connect applications. Since these cards are usually manufactured by third party, the host adapter designer retains little control over the cost of the most expensive components on his adapter. A direct mounting of the transceivers on the host adapter PCB, allows choice of vendor for the expensive transceiver component and allows for a base design which supports the majority copper connection environment. A single board, optimized for copper, may be kept in inventory, and become the basis for any fibre application. This approach provides for the lowest possible cost of entry to fibre channel direct attach.

All that is needed is to provide for a means to adapt optical media for point to point applications exceeding the serviceable distance limits of copper. Such an upgrade can be provided in the form of a pluggable module which contains the necessary optical converters and the connector interfaces to the host and media. It is this approach to media adaptation which this document purports to describe.

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8 Introduction and Scope

The development of the arbitrated loop specification as part of the fibre channel standard has established the importance of direct attach storage applications to the market success of fibre channel. Cost effective solutions to fibre channel direct attach suggest a design approach that facilitates a base host adapter that supports “copper” connections utilizing twinax and coax cabling. Applications requiring optical media are accommodated by the plug in of an external optical converter module, available in the aftermarket.

Copper connections at 1 GHz have been demonstrated to operate at distances up to 30 meters. These operating distances render copper useful to a large majority of storage applications which may benefit from the connectivity and bandwidth advantages inherent with fibre channel technology. Copper is a low cost entry point for fibre channel, making this technology a cost/performance superior alternative. This “entry solution” is thus free of the cost and mechanical burdens associated with approaches such as the GLM.

This document defines the application of the DB-9 (9-pin D-sub connector) as referenced in the fibre channel standard for use as an interface with external plugable modules conforming to a card edge panel mount construction.

This document describes only those external physical and electrical characteristics required to permit vendor interchange in such applications.

The anticipated application of these modules is for conversion of electrical signal to modulated light for transmission on optical media. It is conceivable, however, that in the future other functions such as equalization may be implemented using this approach.

9 Normative References

The following standards, specifications and technical reports are referenced in this specification. At the time of publication, the editions indicated were valid. All standards and specifications are subject to revision, and parties to the agreements based on these standards or specifications are encouraged to investigate the possibility of applying the most recent editions. Members of IEC and ISO maintain registers of currently valid ISO standards. ANSI performs a similar function for American National Standards.

The present keeper of this specification is the DB-9 MIA Adhoc Committee chaired by Norm Harris, at Adaptec Inc., 691 S. Milpitas Blvd., Milpitas, Ca. This adhoc group is open to participation without prejudice to all parties who may have interest in the development of the specification for fibre channel products. It is anticipated that this specification will be remanded to ANSI Committee X3T11 for processing as a technical report upon its completion. Unless otherwise stated in this specification, the provisions of the standards and specifications listed below in this section are normative to this specification.

- **Fibre Channel Physical and Signalling Interface (FC-PH), ANSI X3.230-1994**
- **Fibre Channel Physical and Signalling Interface-2 (FC-PH-2), X3T11/Project 901D/REV 7.3**
- **Fibre Channel Physical and Signalling Interface-3 (FC-PH-3), X3T11/Project 1119D/REV 8.8**
- **Fibre Channel Arbitrated Loop-2, FC-AL-2/Rev 5.1**
- **Fibre Channel Private Loop SCSI Direct Attach /X3T11/Project 1162DT/Rev 1.5**
- **IEC 825-1:1993, Radiation Safety of Laser Products, equipment classification, requirements and user's guide**

10 Definitions and Conventions

10.1 Definitions

10.1.1 Media Interface Adapter

An external plug in module containing a 9-pin D-sub, required electronics, and the necessary connector to adapt to media. This module is rear panel/card edge mountable to the host adapter.

10.1.2 Host

Where used the term host refers to either an intelligent host adapter/controller or a “dumb” stand-alone peripheral or collection of such devices such as disk drives. Dumb peripherals may not implement all control features provided at the DB-9 interface. Instead they rely on upper layer detection of FAULT- conditions.

10.1.3 FAULT-, fault

The lowercase word “fault” where used in this specification refers to a condition of the MIA circuitry or attached media that may cause the assertion of the FAULT- signal at the MIA interface. There are essentially three fault conditions discussed in this specification, the interface fault, a module and a link fault as defined in Clause 4. Where used by itself, the word “fault” refers to the interface fault condition. The word “FAULT-” is used to refer to the electrical signal at the MIA interface.

10.1.4 Host Adapter

An intelligent controller device typically residing on the backplane of a host computer.

10.2 Abbreviations, acronyms and symbols

10.2.1 MIA

Media Interface Adapter.

10.3 Editorial Conventions

In the case of any conflict between figure, table, and text, the text takes precedence. Exceptions to this convention are indicated in the appropriate sections.

The term “shall” is used to indicate a mandatory rule.

The term “should”, “may” or “optionally” is used to indicate a choice that may be made by the implementor.

Where not explicitly stated otherwise, all existing fibre channel and optical standards and specifications as listed in section 2.0, Normative References, shall apply to the implementation of this specification.

11 Interface Functional Description

11.1 Interface Pinout definition

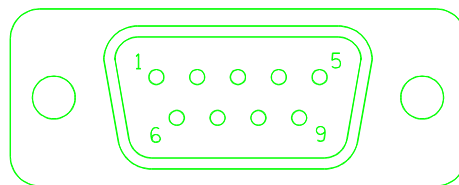
The following table defines interface pin assignment. The column headed "IN/OUT" is the direction of signal flow specified with respect to the Media Interface Adapter.

Table 1: Interface Pinout Assignment (5 Volt Operation)

Pin No.	Signal Name	IN/OUT	Signal Type	Signal Description
1	Tx+	in	High speed	Differential transmit data in
2	V _{CC}	in	N/A	Power supply, nominal 5 Vdc
3	FAULT-	out	Control level	Module fault detect
4	KEY	N/A	N/A	Mechanical key position
5	Rx+	out	High speed	Differential receive data out
6	Tx-	in	High speed	Differential transmit $\overline{\text{data in}}$
7	ODIS+	in	Control level	Optical output disable
8	GND	in	N/A	Signal ground
9	Rx-	out	High speed	Differential receive $\overline{\text{data out}}$
	shield			d-sub metallized shell connected

Figure 1 shows the pin out numbering convention for male mating half of the DB-9. Note that the numbering convention for the female half would be transposed with pin 1 becoming pin 5 and pin 6 becoming pin 9 when the connector is viewed from this perspective.

Figure 1: DB-9-pin Numbering Conventions (Male Connector)



11.2 Description of Interface Signals

11.2.1 Tx+, Tx-

Differential transmit data into the MIA receivers. The electrical signal levels shall be PECL swings as defined in FC-PH.

11.2.2 Rx+, Rx-

Differential receive data out from the MIA drivers. The electrical signal levels shall be PECL swings as defined by FC-PH.

11.2.3 ODIS+

Active high optical output disable signal. This signal is driven by the host.

While asserted, the MIA module shall disable all laser light output. (Due to safety considerations, the optical output may already have been disabled as a result of a detected module fault.). The rising edge of ODIS shall clear any pre-existing latched module fault (refer to section 4.2.4 for a definition of module fault). Section 5.0 defines the interface timing and control and illustrates typical operation of ODIS.

The module shall provide a pullup resistor from ODIS+ to V_{CC} . This pullup resistor value shall be determined by module type. Optionally the host may use this resistor value as a basis for implementing circuitry that permits host identification of the MIA module type. The base values for these pullup resistors shall be 10 k Ω for shortwave laser and 5.1 k Ω for a longwave laser module. The actual resistance shall be within $\pm 7\%$ of these base values over the full operating temperature range of the MIA. Base values of 3.2 k Ω and 2.43 k Ω , with a worst case tolerance of $\pm 2\%$, are reserved for future types.

There may be additional current from other (non-pullup) related sources at the ODIS interface due to functional logic inputs in the MIA. Stated limits on this current shall apply over the full range of MIA operating temperature and V_{CC} . For all input voltage (V_{in}) between 0V and 0.4V, the logic low input current shall not exceed the current which would flow in a 20 k Ω resistor between V_{in} and V_{CC} (e.g. -250 μ A @ $V_{CC} = 5V$, $V_{in} = 0V$.) For all V_{in} between 2.4V and V_{CC} , the logic high input current shall not exceed the current which would flow in a 50 k Ω resistor from V_{in} to ground (e.g. + 50 μ A @ $V_{in} = 2.5V$)

Optionally the host may implement circuitry that provides for host detection of module type. This may be accomplished on the host by performing an appropriate voltage or current sensing scheme on the ODIS signal line. The design and specification of this circuitry is beyond the scope of this specification.

11.2.4 FAULT-

Active low signal. FAULT- is the logical NOR that a module fault or link fault condition has been detected. This signal is driven by the MIA module.

A module fault shall be defined as the failure of the optical output of the MIA. As a minimum, the assertion of FAULT- indicates that one or both of the following operational conditions have been detected. (1) laser end-of-life—the laser control circuitry is no longer capable of providing sufficient bias current to sustain adequate optical output power to provide reliable transmission over the link and/or (2) single point of failure in the laser servo control circuitry—the laser servo control has failed and the monitor circuitry has detected the condition. A module fault shall be latched. A module shall assert FAULT- on when either condition (1) or (2) has been detected.

A module fault shall be cleared on the rising edge of ODIS, and shall remain deasserted for the duration of the assertion of ODIS.

A link fault shall be defined as a loss of signal on the incoming link. A link fault shall cause the assertion of FAULT- until the loss of light condition has been cleared. Signal detect or LOL functions shall be implemented per the guidelines given in clause 5.6 of FC-PH, X3.230-1994.

The host shall provide a pull up resistor to V_{CC} in the range of 4.7 k Ω to 10.0 k Ω .

This signal shall have TTL/CMOS levels as defined in section 6.4.

FAULT- may be implemented using an open-collector or open-drain output.

Section 5.0 details critical timing values and illustrates typical operation of the FAULT- signal.

11.2.5 KEY

This pin on the interface shall be plugged on the host side to prevent installation of DB-9 assemblies not intended for this application. The MIA connector shall not have a pin installed in this position. This pin position shall have no electrical function.

11.2.6 V_{CC}

Regulated power supply provided by the host. Power requirements are defined in section 6.4. NOTE: Modules requiring more than $I_{CC\ max}$ shall have V_{CC} supplied from an external source. If external power is supplied, the MIA shall draw no power through the DB-9 host interface.

11.2.7 Gnd

Isolated signal ground. There shall be no connection of this GND to chassis or to the DB-9 connector shell within the MIA.

11.3 Enclosure Grounding Requirements

Both mating parts of the DB-9 shall have a conductive shell. The host mating part shall secure the conductive shield to the HOST chassis. If the MIA has any exposed conductive surfaces, those surfaces shall have a conductive path of DC resistance no greater than $0.3\ \Omega$ to the host chassis when connected to the host DB-9 connector.

12 Interface Timing Specifications and Examples

12.1 Interface Timing Values

Table 2: Interface Timing Values

Symbol	Min	Max	Units	Description
$t_{pw_fault_reset}$	100		ns	minimum ODIS assertion time to clear a module fault condition
$t_{pd_modfault_ON}$		1	ms	delay from laser over power module fault detect to FAULT- assertion
t_{pd_ON}		2	ms	laser on time from deassertion of ODIS
t_{pd_OFF}		2	ms	laser off time from assertion of ODIS
$t_{pd_LOL_OFF}$		2	ms	delay from deassertion of LOL condition to deassertion of FAULT-
$t_{pd_LOL_ON}$		2	ms	delay from assertion of LOL condition to assertion of FAULT-
$t_{pd_FAULT_reset}$		1	μ s	delay from assertion of ODIS to clear of FAULT-

12.2 Host Servicing of MIA Fault Conditions

The FAULT- signal shall be asserted on the MIA interface when either a link fault or a module fault condition exists.

It is recommended that the host periodically sample the state of the FAULT- signal as opposed to rely on the high-to-low transition of FAULT- to detect a fault condition. The assertion of ODIS does not clear an outstanding link fault condition. If a “compound” fault condition exists, where both a link fault condition proceeded by a module fault condition occurs (reference figure 4), the link fault will not generate a low going transition on FAULT-.

Upon the initial detection of the assertion of FAULT-, the host shall attempt to clear FAULT- only once through the assertion of ODIS.

Service routines shall interpret the interface fault condition as follows. Refer to the timing specifications as given in Table 2.

Upon detecting the assertion of FAULT-, the host shall first sample FAULT- at the MIA interface. If FAULT- is not asserted, the host shall report the fault condition as a self corrected link fault. If FAULT- is asserted, the host shall assert ODIS, wait of minimum of $t_{pd_FAULT_reset}$, and sample the state of FAULT-. If FAULT- remains asserted, the host shall release ODIS, report the outstanding fault condition as a link induced fault and revert to the servicing of an outstanding link fault condition as suitable for the target application.

If FAULT- is cleared during the assertion of ODIS, the host shall report the fault condition as a module

induced fault. The host shall release ODIS after a minimum of $t_{pd_FAULT_reset}$, wait a minimum of t_{pd_ON} and sample the state of FAULT-. If FAULT- is asserted, the host shall report a hard module failure condition. If FAULT- is cleared, then the module fault condition has been corrected and the link has resumed normal operation.

12.3 Typical Interface Operation for Module Fault Condition

Figure 2 illustrates typical interface operation for the event of a module fault condition.

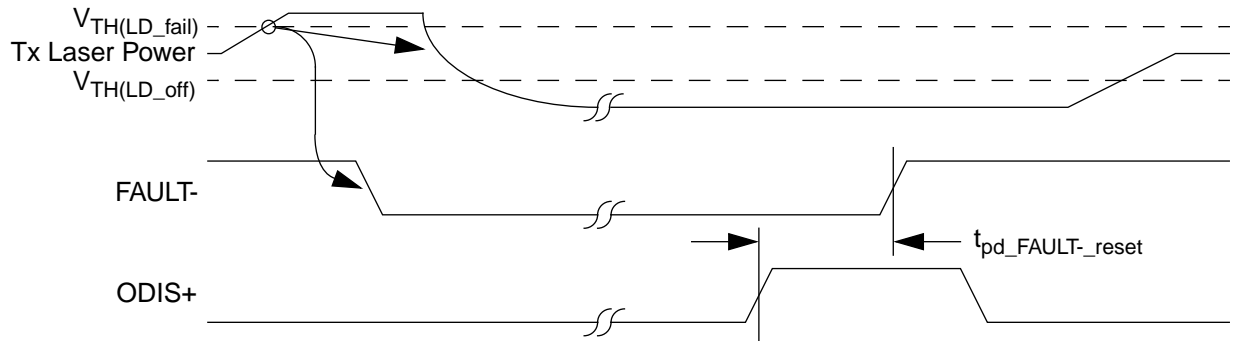


Figure 2: Module Fault interface timing Example

12.4 Typical Interface Operation for Link Fault Condition

Figure 3 illustrates interface operation for a typical link fault condition.

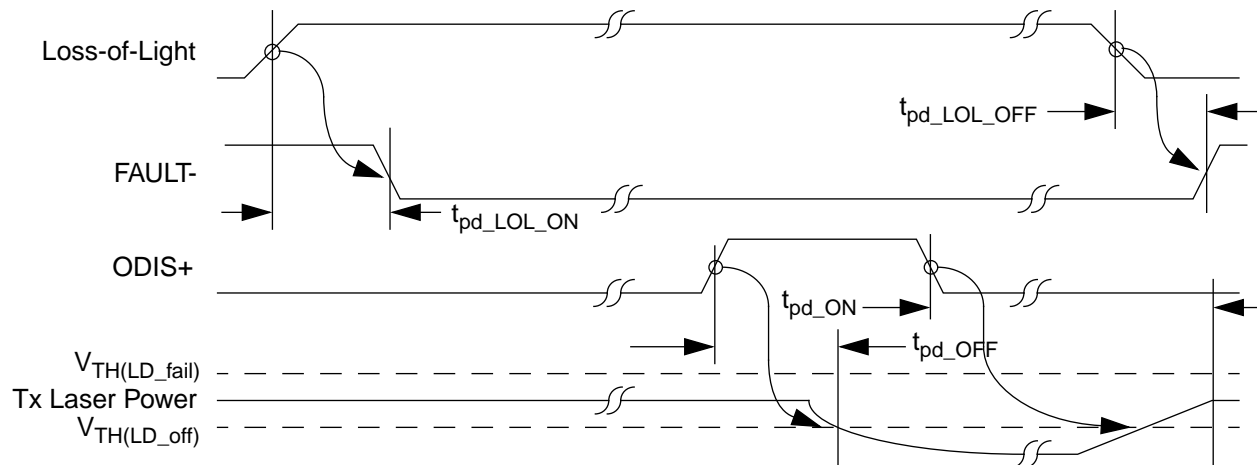


Figure 3: Typical Interface Operation for Link FAULT- Event

12.5 Typical Interface Operation-Combined Module and Link Fault

Figure 4 illustrates the operational scenario for the event of a combined module and link fault.

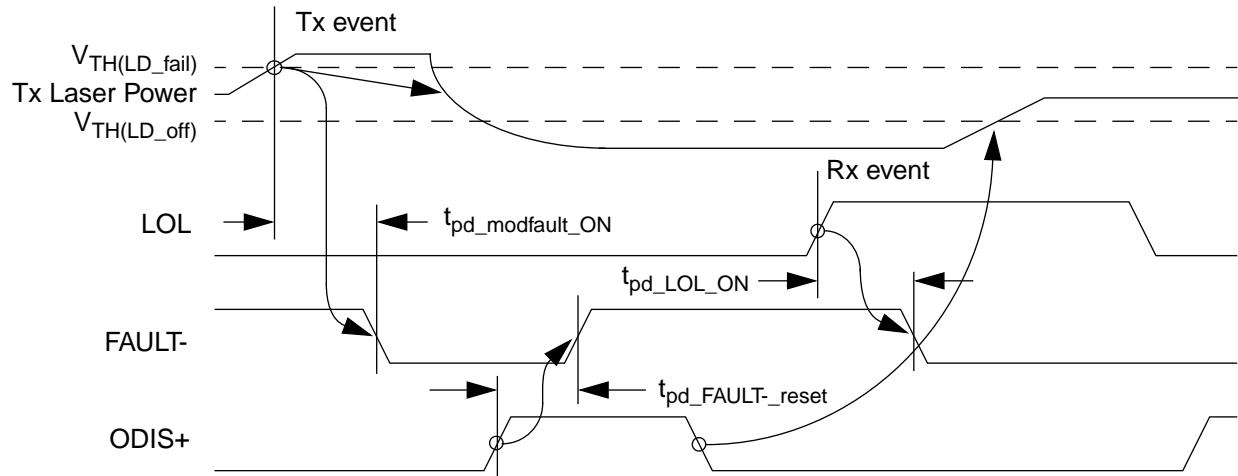
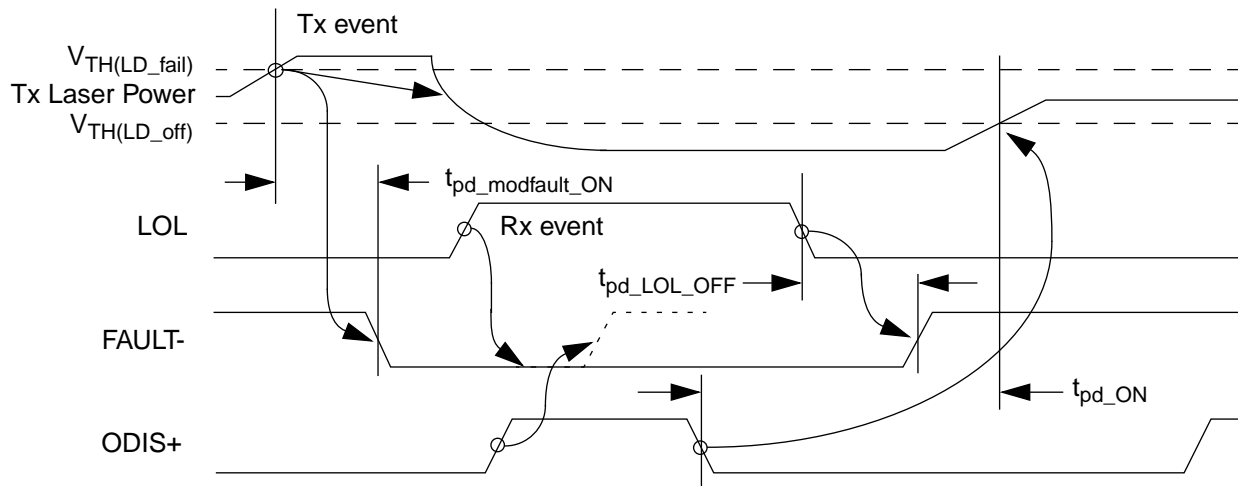


Figure 4: Typical operation-Combined module and link fault event



note: the assertion of ODIS clears only the module fault condition. FAULT- will remain asserted until the LOL condition is cleared.

Figure 5: Typical operation-Pre-existing module fault followed by link fault (LOL) condition

12.6 Typical Interface Operation-Power On Event

Figure 5 illustrates typical interface operation during power on and hot plugging events.

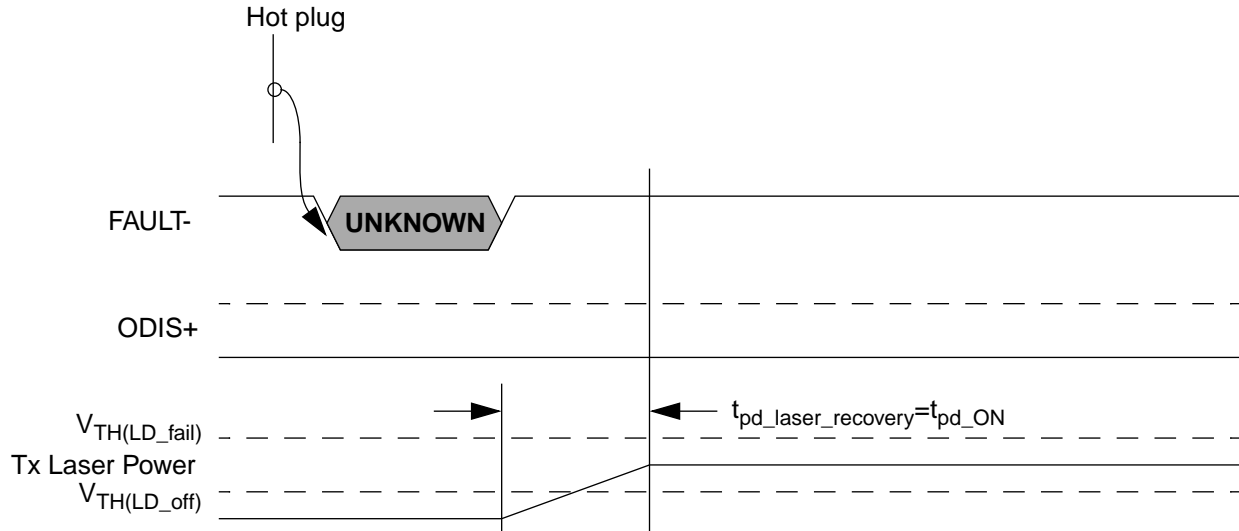


Figure 6: Power on and Hot Plug Operation

12.7 Host Operation Requirements Non Intelligent MIA Interface

Host implementations which do not desire hardware control of the MIA fault mechanism may optionally ignore the FAULT- signal and ground the ODIS signal output at the MIA interface. IT IS RECOMMENDED/REQUIRED TO INSURE PRODUCT INTERCHANGEABILITY, THAT ALL MIA HARDWARE WILL ATTEMPT RESTART OF THE LASER IF THE CONDITION CAUSING THE FAULT IS SELF CLEARING. This will permit MIA usage with nonintelligent peripherals and hosts desiring software control of the interface.

13 Electrical Interface Requirements

13.1 Environmental/FCC

Environmental specification shall be as required by the application operating environment. It is recommended that the MIA be qualified for operation at FCC Class B.

13.2 Laser Safety Requirements

The MIA shall conform to all provisions for laser safety as provided for in IEC 825-1.

13.3 Hot Plugging Considerations

For eye safety practices it is recommended practice that a fibre optic cable be attached to the MIA prior to plugging it into a powered connection.

13.4 Power

Power shall be supplied by the host to pin (2) of the interface designated V_{CC} . The host shall supply fused power to the DB-9 interface. Maximum permissible inrush current shall be 4 amps over 50 μ s. (specified as the duration of maximum peak current above the maximum supply current I_{CC} as defined in table 3). Voltage and current operating ranges are listed in the following table.

Table 3: Interface Electrical Power Requirements

Parameter	Symbol	Min	Typical	Max	Units
Supply voltage	V_{CC}	4.5	5.0	5.50	V
Supply Current	I_{CC}			250	mA

13.5 High speed signalling levels

Those signals designated high speed shall operate at PECL swings and impedance levels as defined within FC-PH. High speed signals shall be AC coupled on the host side of the connection as specified in FC-PH. High speed signals may use series resistance damping as required in an application. Care should be taken to provide at least a 600mv peak-to-peak signal swing output under damped conditions.

13.6 Control signal level

Those signals at the MIA interface specified as control signal levels shall be as defined in the following table.

Table 4: TTL/CMOS Control Signal Levels

Symbol	Parameters	Conditions		Min	Typ	Max	Units
V_{OH}^1	Output High Voltage	$I_{OH} = -400\mu A$	$V_{CC} = \text{min}$	2.4	3.0	V_{CC}	V
V_{OL}	Output Low Voltage	$I_{OL} = 4 \text{ mA}$	$V_{CC} = \text{min}$	0	0.25	0.6	V
V_{IH}	Input High Voltage			2.0	-	5.5	V
V_{IL}	Input Low Voltage			0	-	0.8	V
I_{IH}	Input High Current	$V_{CC} = \text{Max}$	$V_{IN} = 2.4V$		-	40	μA
I_{IL}	Input Low Current	$V_{CC} = \text{Max}$	$V_{IN} = 0.4V$	-	-	-4	ma
C_{IN}	Input capacitance					15.0	pf
t_R^2	Control level rise time	0.8V to 2.0V		0.7	-	10.0	ns
t_F^2	Control level fall time	2.0V to 0.8V		0.7		10.0	ns

¹ I_{OH} not applicable in the case of open-collector or open-drain output

² Minimum specifications do not apply to open-collector or open-drain implementations

14 Mechanical Specifications

14.1 Module dimensions

The following dimensions are given as maximum dimensions for the MIA. It is recommended that the length dimension be kept as short as possible to provide for adequate clearance in an “inside the cabinet” installation of the MIA. The height and width dimensions have been specified so as to permit side-by-side and the mounting of two DB-9 connectors within the standard PCI, VME and Multibus slot dimensions.

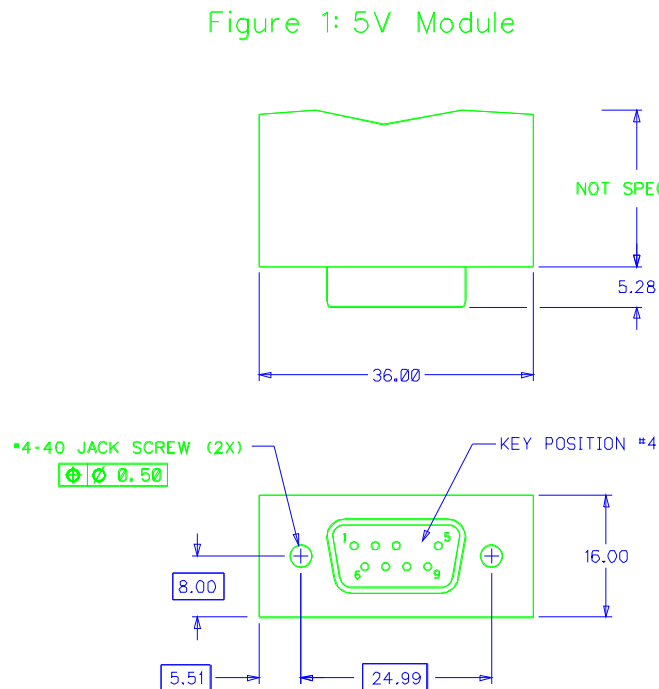
Maximum height: 36.00 mm

Maximum width: 16.00 mm.

Maximum length: 90.0mm

Figure 7 illustrates these requirements.

FIGURE 7-MIA Module Dimensions



14.1.1 Connector Location Requirements for MIA

Figure 7 shows the permissible mounting region for the DB-9 female connector assembly referenced to the maximum footprint as defined in 7.1. Location of the connector within this region will provide adequate side clearance in applications which require side by side mounting of MIA assemblies.

14.2 Connector definitions

The connector used for the host to module mating interface shall be a 9-pin D-subminiature of the genders described below. The module shall have a jack screw retention mechanism mounted on dimensions as shown in Figure 7.

14.2.1 Keying Requirements

Connector pin 4 shall be designated a key.

14.2.2 Host connector description

The host connector shall be a 9-pin D-sub female. A mechanical key shall be implemented on the connector by blockage of pin 4.

14.2.3 Module mating interface to host

The module mating interface connector shall be a male 9-pin D-sub connector. Pin 4 shall be removed to facilitate mating with any host female DB-9 intended for this application.

14.2.4 Module mating interface to media

The mating interface on the media side shall be specific to the application and is not defined by this specification. Note: The optical module typically referred to in this specification uses the SC type full duplex connector as described in the fibre channel standard, FC-PH, X3.230-1994.